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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,896	11/20/2003	Yung-Chang Lin	JCLA11793	1665

23900 7590 07/25/2006

J C PATENTS, INC.
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IRVINE, CA 92618

EXAMINER	
VU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,896	LIN ET AL.	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.914

1. A request for continued examination under 37 CFR 1.114, including the, fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/05/06 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13-17 and 25-36 are rejected under 35 U. S. C. 102(b) as being anticipated by Rajeevakumar (US Pat. 5,426,324).

Regarding claims 13, 14, 16, 17 and 34-36, Rajeevakumar discloses in figs. 1, 8 and 13 a trench capacitor, comprising: a substrate 1 having a trench; a conducting layer 11 filling trench; a first capacitor dielectric layer 10 between a surface of trench and conducting 11; a protruding

electrode 2 on substrate 1 around trench and covering a junction of trench and substrate 1; a second capacitor dielectric layer 4a (fig. 8) between conducting layer 11 and substrate 1, substrate 1 around first and second capacitor dielectric layers 10/4a being a bottom electrode; and a conducting structure electrically 8 (col. 2, lines 43-58) connecting protruding electrode 2 and conducting layer 11, wherein conducting layer 11, protruding electrode 2, and conducting structure 8 serve as an upper electrode, and wherein conducting structure 8 electrically connecting protruding electrode 2 by contacting the upper surface of protruding electrode 2 (fig. 1).

Regarding claims 25, 26, 28, 29, Rajeevakumar discloses a dynamic random access memory cell, comprising: a substrate 1 having a trench; a conducting layer 11 filling trench; a first capacitor dielectric layer 10 between the surface of trench and conducting layer 11, a protruding electrode 2 on substrate 1 around trench and covering a junction of trench and substrate 1; a second capacitor dielectric layer 4a between conducting layer 11 and substrate 1, substrate 1 around first and second capacitor dielectric layers 10/4a being a bottom electrode; a gate electrode 2 on substrate 1 beside protruding electrode 2; a plurality of drain/source regions 13 in substrate beside two sides of gate electrode 2; a gate dielectric layer 4a between gate electrode 2 and substrate 1; and a conducting structure 8 electrically connecting protruding electrode 2 (fig. 1) and conducting layer 11, and conducting layer 11, protruding electrode 2, and conducting structure 8 (col. 2, lines 43-58) being an upper electrode, and wherein conducting structure 8 electrically connecting protruding electrode 2 by contacting the upper surface of protruding electrode 2 (fig. 1).

Regarding claims 15, 27, 32 and 33, Rajeevakumar discloses capacitor dielectric layer comprises: a first portion 10 (col. 3, lines 8-27 and 58-65) between the surface of trench and conducting layer 11; and a second portion 4a (col. 4, line 27) between conducting layer 11 and substrate 1 (fig. 8).

Regarding claim 30, Rajeevakumar discloses a plurality of spacers 4 on sidewalls of conducting layer 2 and gate electrode 2 (fig 8)

Regarding claim 31, Rajeevakumar discloses a self-aligned silicide layer 14 on surfaces of conducting layer 11 and gate electrode 2 (fig. 1).

3. Claims 18-24 are rejected under 35 U. S. C. 102(b) as being anticipated by Jeon (US Pat. 5,455,192).

Jeon discloses in figs. 3 and 4E-4G a dynamic random access memory cell, the memory cell comprising: a substrate 40 having a trench; a conducting layer 64 filling trench and extending to substrate 40 around trench; an ONO capacitor dielectric layer 62 between a surface of trench and conducting layer 64, and between conducting layer 64 and substrate 40, conducting layer 64 being an upper electrode, and substrate region 60 around capacitor dielectric layer 62 being a bottom electrode, wherein the ONO capacitor dielectric layer 62 continuously extends from inside the trench to an upper surface of the substrate; a gate electrode 50 on substrate 40 beside conducting layer 64; a plurality of drain/source regions 52/53 in substrate beside two sides of gate electrode 50; and a gate dielectric layer 48 between gate electrode 50 and substrate 40.

Response to Arguments

4. Applicant's arguments with respect to claims 13-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith S can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAVID VU
PRIMARY EXAMINER